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Claim Objections

In paragraph 4 of the Office Action, the Examiner objects to claims 1 and 7 because of alleged informalities in the claims. Applicant has amended the claims per the Examiner's suggestion to overcome these objections. The claims as amended are believed to be in allowable condition.

Rejection under 35 U.S.C. §112

In paragraph 5 of the Office Action, claims 3-5 are rejected under 35 U.S.C. §112, second paragraph, as being indefinite for allegedly failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Applicant has amended the claims per the Examiner's suggestion to overcome these rejections. The claims as presented are believed to be in allowable condition.

Rejections Under 35 U.S.C. §103(a)

Claims 1-6 and 8 are rejected under 35 U.S.C. §103(a) as being unpatentable over Orihara et al. (U.S. Patent No. 5,705,852) in view of Fidalgo (U.S. Patent No. 5,671,525). Applicant respectfully traverses this rejection, as the Office Action fails to set forth a prima facie case of obviousness, and the references teach away from the combination.

1. <u>Discussion of the Cited References</u>

A. Orihara

Orihara discloses a non-contact integrated circuit (IC) card which comprises a substrate, an antenna formed on the substrate by etching, and a chip connected to the antenna with an anisotropic conductive adhesive layer (Abstract). Orihara teaches that employing an anisotropic conductive layer to connect the chip and the antenna produces an IC card that is not too thick, has high connection reliability and low material and production costs (col. 3, lines 33-39), and makes connection wires unnecessary (col. 4, lines 1-2).

To produce the IC card, Orihara forms the anisotropic layer on top of the antenna and places a fully assembled chip on top of the layer. Orihara teaches that a desirable thickness of the anisotropic layer is between 10 and 50 micrometers (col. 5, lines 21-24), and that connecting "bumps" on the IC chip may be connected to the antenna coil via the anisotropic conductive

layer by heating or exposure to ultraviolet rays (col. 5, lines 49-52). After connection is achieved, the completed card is produced by coating the substrate with a urethane resin, and then placing the coated substrate between insulating films of polyethylene terephthalate or other thermoplastic covering on both sides (col. 5, lines 1-4). In this manner, a non-contact IC card with a thickness of 0.76 mm is produced (col. 6, lines 24-25). As is discussed below, Fidalgo states that a card of this thickness complies with the ISO 7810 standard (col. 1, lines 29-31).

B. Fidalgo

Fidalgo discloses an IC card produced by forming a cavity in a card body into which an antenna has been laid, mounting an electronic module (including a chip) in the cavity, and connecting the electronic module to the antenna (Abstract). Because Fidalgo discloses a hybrid IC card (i.e., one which communicates with a reader via either contact or contact-free communication), the mounting step also includes exposing a series of pads 11 that will contact a reader on the outer surface of the card 4 (Abstract). The chip 8 sits directly below and flush against the outside of the card 4 (col. 3, lines 39-42), fixedly set within a quantity of protective resin 14 that fills the remaining space in the cavity (col. 3, lines 65-67). The chip 8 is connected to the antenna 5 via wires 9 or conductive tape that is affixed to one of several contact zones 12 (see Fig. 1, col. 3, lines 59-64). After the electronic module is mounted in the cavity, the entire structure is given upper and lower thermoplastic coverings 3,4 similar to that employed by Orihara (col. 5, lines 5-9). The cavity extends nearly the entire thickness of the card between thermoplastic covering layers 3, 4 (Fig. 1). Therefore, the distance between Fidalgo's chip and the antenna is almost the entire thickness of the card. Fidalgo states that card thickness meets the ISO 7810 standard of 0.76 mm (col. 1, lines 29-31, col. 4, lines 53-54).

2. The Office Action Fails to Set Forth a Prima Facia Case of Obviousness

The rejection of claims 1-6 and 8 under 35 U.S.C. §103(a) is improper because the Office Action has failed to establish a *prima facie* case of obviousness.

According to MPEP §2141.01(a), it is essential that some motivation or suggestion be found for the combination of the references. MPEP §2142 further states that the Office Action must provide some suggestion of the desirability of the claimed invention to support a conclusion of obviousness.

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In paragraph 7, the Office Action makes numerous assertions as to why it allegedly would have been obvious to incorporate the teachings of Fidalgo to improve the IC card of Orihara. None of these are supported by the prior art of record.

First, the Office Action asserts that one skilled in the art would have been motivated by Fidalgo to place the chip of Orihara in a cavity, so as to reduce the thickness of the resulting IC card. This assertion is not supported by either Orihara or Fidalgo. The prior art of record (e.g., Fidalgo) discloses that the ISO 7810 standard for the thickness of IC cards is 0.76 mm, which both Orihara (col. 6, lines 24-25) and Fidalgo (col. 1, lines 29-31) have achieved. Furthermore, Orihara states that he has achieved a desirably compact system (col. 3, lines 37-38). Thus, the prior art of record does not teach any desirability of decreasing the thickness of the card in Orihara, as doing so would produce a card too thin to comply with the ISO standard. Thus, the alleged motivation of seeking to reduce the thickness of the card in Orihara is entirely unsupported in the prior art of record. In fact, both references actually teach away from reducing the thickness of the Orihara card.

Second, the Office Action asserts that one skilled in the art would have been motivated by Fidalgo to place the chip of Orihara in a cavity because doing so would reduce the amount of adhesive required. Again, this contention is not supported by the references. Modifying Orihara to place the chip in a cavity would, at a minimum, require adhesive to be placed around the sides of the chip in the cavity (rather than simply along the bottom face of the chip), thereby actually increasing the amount required (see Fig. 1B of Orihara). Fidalgo states that his cavity is completely filled with adhesive (col. 3, lines 65-67). Given that Fidalgo's cavity extends nearly the entire distance between upper and lower protective sheets 3, 4 (see Fig. 1), the adhesive needed to fill this cavity is obviously more than Orihara employs. Thus, this alleged motivation for modifying Orihara based on Fidalgo is unsupported by the prior art of record.

Third, the Office Action asserts that one skilled in the art would have been motivated to modify Orihara according to the teachings of Fidalgo to reduce the cost of manufacturing the card. This contention is also without support in the prior art of record. Fidalgo does not state that his manufacturing process is a more cost-effective method of producing IC cards than that employed in Orihara. Also, as discussed above, modifying Orihara according to the teachings of Fidalgo would require more adhesive, thus increasing material costs. Thus, this alleged

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motivation for modifying Orihara based on Fidalgo is also entirely unsupported by the prior art of record.

Fourth, the Office Action asserts that modifying Orihara to place the chip in a cavity according to Fidalgo would provide the chip with better protection. This contention is also without support in the references. The Orihara chip is secure, as it is embedded within a large quantity of core material 9 that sits between upper and lower resin films 10 (see Fig. 6E) such that one skilled in the art would not be motivated to modify Orihara to better secure the chip. In addition, Fidalgo places the chip directly behind contact pads 10, 11 that sit flush against the outside of the card, so as to facilitate contact with a reader (see Fig. 1, col. 3, lines 39-42). Thus, modifying Orihara according to Fidalgo could only provide the chip with less protection. The alleged motivation for modifying Orihara based on Fidalgo is unsupported by the prior art of record.

In sum, none of the contentions made in the Office Action to provide alleged motivation for modifying Orihara based on Fidalgo are supported in the prior art of record. Thus, the Office Action fails to set forth a prima facie case of obviousness, such that the rejection of claims 1-6 and 8 under 35 U.S.C. §103(a) should be withdrawn.

3. The References Teach Away From the Combination

Rather than providing motivation for the combination, the cited references actually teach away from the combination alleged in the Office Action.

Orihara teaches that an IC card is produced with low material cost by employing an anisotropic conductive layer to connect the chip with the antenna (col. 3, lines 34-37, col. 4, lines 7-9). Orihara also describes a desirable amount of anisotropic adhesive to be placed between the chip and the antenna (col. 5, lines 21-25; see also Fig. 1B). Fidalgo, however, teaches that the chip is fixedly set within a quantity of protective resin 14, wherein the resin completely fills a cavity that extends the approximate distance between the upper and lower surfaces 3, 4 (see Fig. 1, col. 3, lines 65-67). Thus, modifying Orihara by placing the chip in a cavity according to Fidalgo would require doing one of three things: (1) maintaining the distance prescribed by Orihara between chip and antenna, but enclosing the chip with more adhesive; (2) increasing the distance between chip and antenna, by placing more adhesive than Orihara prescribes; or (3) doing both. Any of these solutions would increase the amount of adhesive used and increase the

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card's material costs. Orihara teaches that a low material cost is desirable. Thus, Orihara teaches away from the combination.

Because Orihara teaches away from the combination, the rejection of claims 1-6 and 8 under 35 U.S.C. §103(a) should be withdrawn for this additional reason.

CONCLUSION

In view of the foregoing amendments and remarks, this application should now be in condition for allowance. A notice to this effect is respectfully requested. If the Examiner believes, after this amendment, that the application is not in condition for allowance, the Examiner is requested to call the Applicant's attorney at the telephone number listed below.

If this response is not considered timely filed and if a request for an extension of time is otherwise absent, Applicant hereby requests any necessary extension of time. If there is a fee occasioned by this response, including an extension fee, that is not covered by an enclosed check, please charge any deficiency to Deposit Account No. 23/2825.

Respectfully submitted, Guillaume Royer, Applicant

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Docket No. S01022.80246.US Date: January 33, 2003

or to a to a

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MARKED-UP CLAIMS

Claims 1, 3, 4, 5 and 7 have been amended as follows:

- 1. (Amended) An electronic circuit including a planar base <u>having first and second</u> <u>base surfaces</u>, an antenna attached on [a] <u>the</u> first surface of the base, and a chip connected to the antenna, characterized in that a double faced adhesive is glued on one of the base surfaces, a slot being made in the double faced adhesive and the chip being arranged at least partially in [this] <u>the</u> slot.
- 3. (Amended) The electronic circuit of claim 1, wherein [the] <u>an</u> etched surface of the chip faces the first surface of the base, and the chip is connected to the antenna by welding beads.
- 4. (Amended) The electronic circuit of claim 1, wherein [the] <u>an</u> etched surface of the chip faces the back of the first surface of the base, the chip is placed in a slot made through the base, and the chip is connected to the antenna by welding beads, the chip being attached to the base by a drop of resin.
- 5. (Amended) The electronic circuit of claim 1, wherein [the] <u>an</u> etched surface of the chip faces the back of the first surface of the base and the chip is connected to the antenna by welding beads located in connection slots going through the base, the chip being attached to the base by a drop of resin.
- 7. (Amended) The electronic circuit of claim 1, wherein the surface of the base which does not receive the double faced adhesive is provided to receive [the] printing of a pattern, of a text or of a code.